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AIDA Electronics

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Systems

Trace Capture

Post processing

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Systems

Bare development FEE64 in T9 has been used to understand the trace capture VHDL.

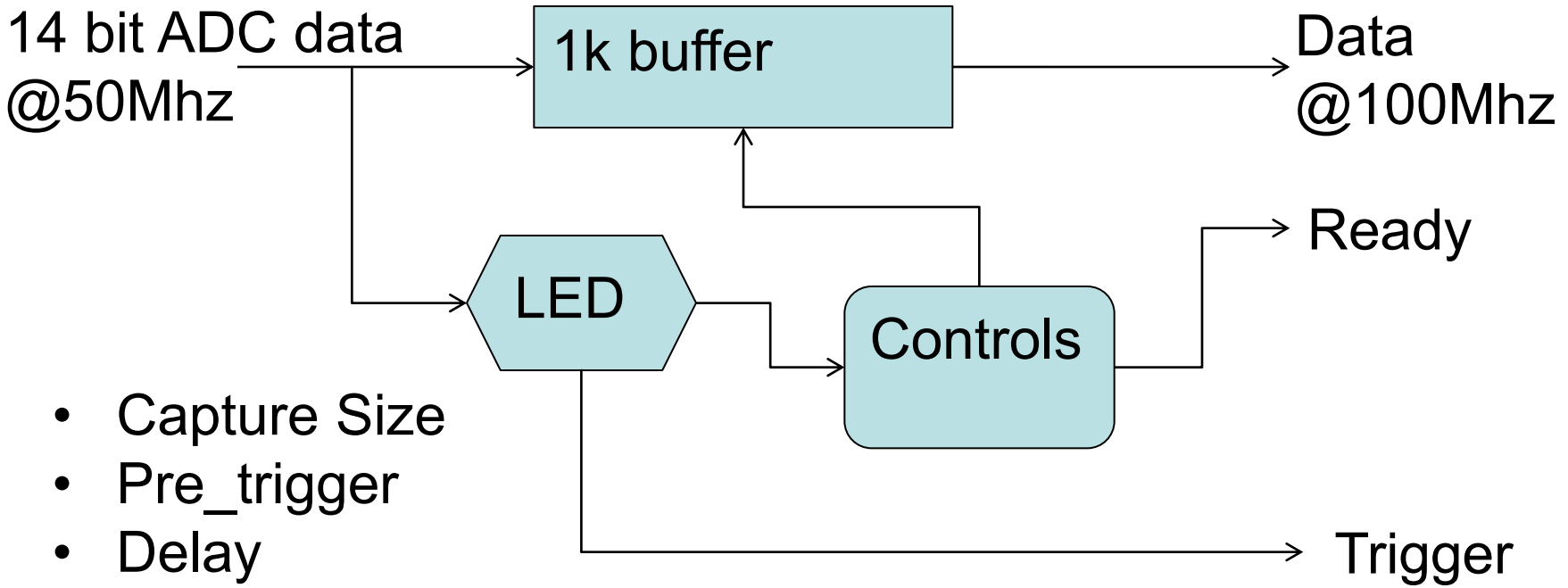
The water cooled 3 slot crate in T9 is used for system software development, trace capture and post processing development and testing. The Edinburgh chiller used for this system failed due to growth of “grot” in the pipework which clogged up the pipes in the chiller. This has been repaired by Technology. This chiller has been sent for use by an Edinburgh experiment. A replacement will be installed soon.

The AIDA structure in T4 is being prepared for system testing with the large chiller and a minimum of a one crate. The intention is to have a full experimental system available for testing and possible experiments.

Trace Capture

- ADC data transfer DDR serial link calibration developed by Mos has been installed and works very reliably on all 64 channels.
- Each of the 64 channels has a Leading Edge Discriminator and a 1024 deep sample memory. Traces are captured to the memory with a Pre_trigger amount of samples defined by the user. Capture size and pre_trigger are common to all channels.
- A group of 8 channels are read out to a single queue. These 8 queues are read out and transferred via DMA to the Linux PPC's main memory. This structure fits in the FPGA taking about an hour to compile with 75% of resources used.
- There is channel deadtime depending on the data rates in the groups and the capture size. This will be explored once the Trace data sorting has been implemented.

Trace Capture - Channel



- Capture Size
- Pre_trigger
- Delay
- Threshold
- Polarity
- Enable

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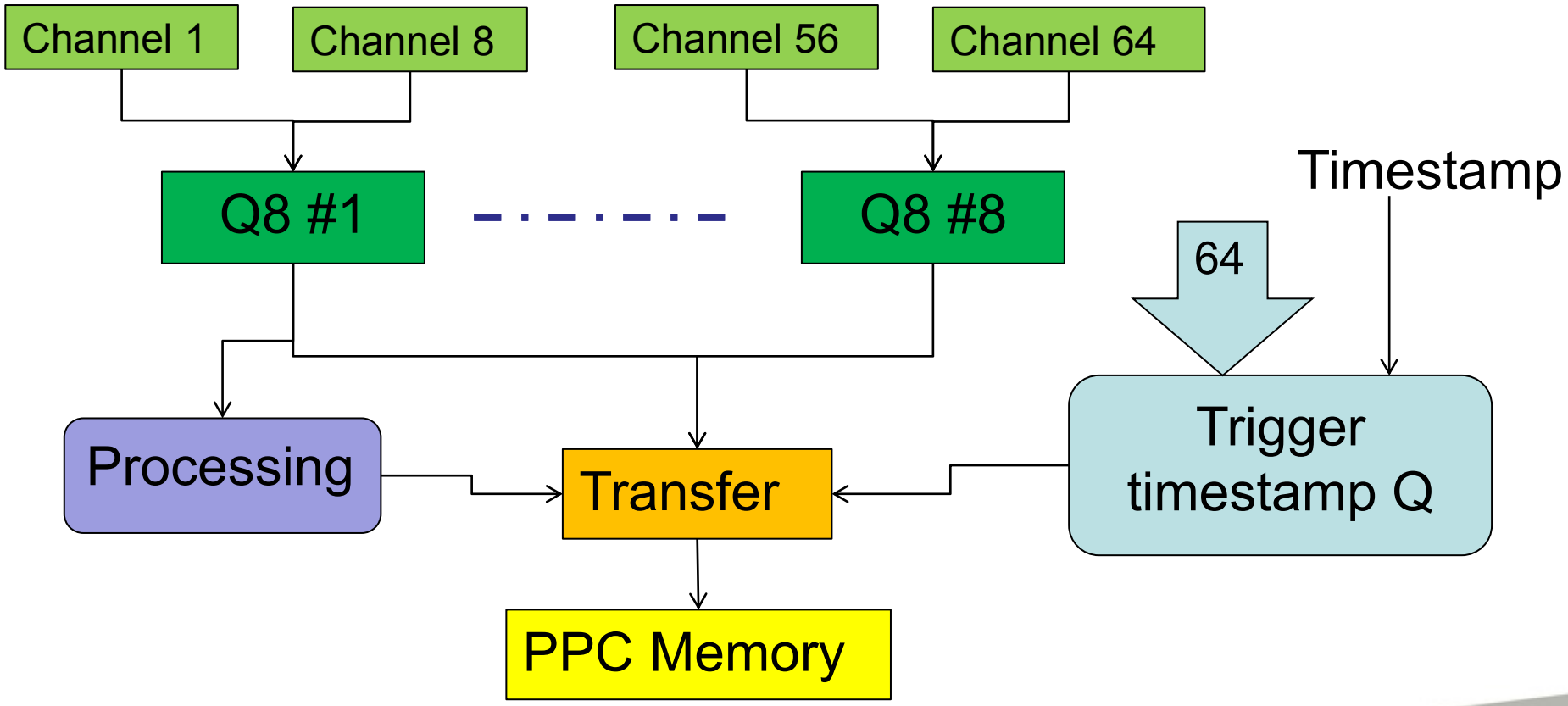
Trace Capture – Readout path



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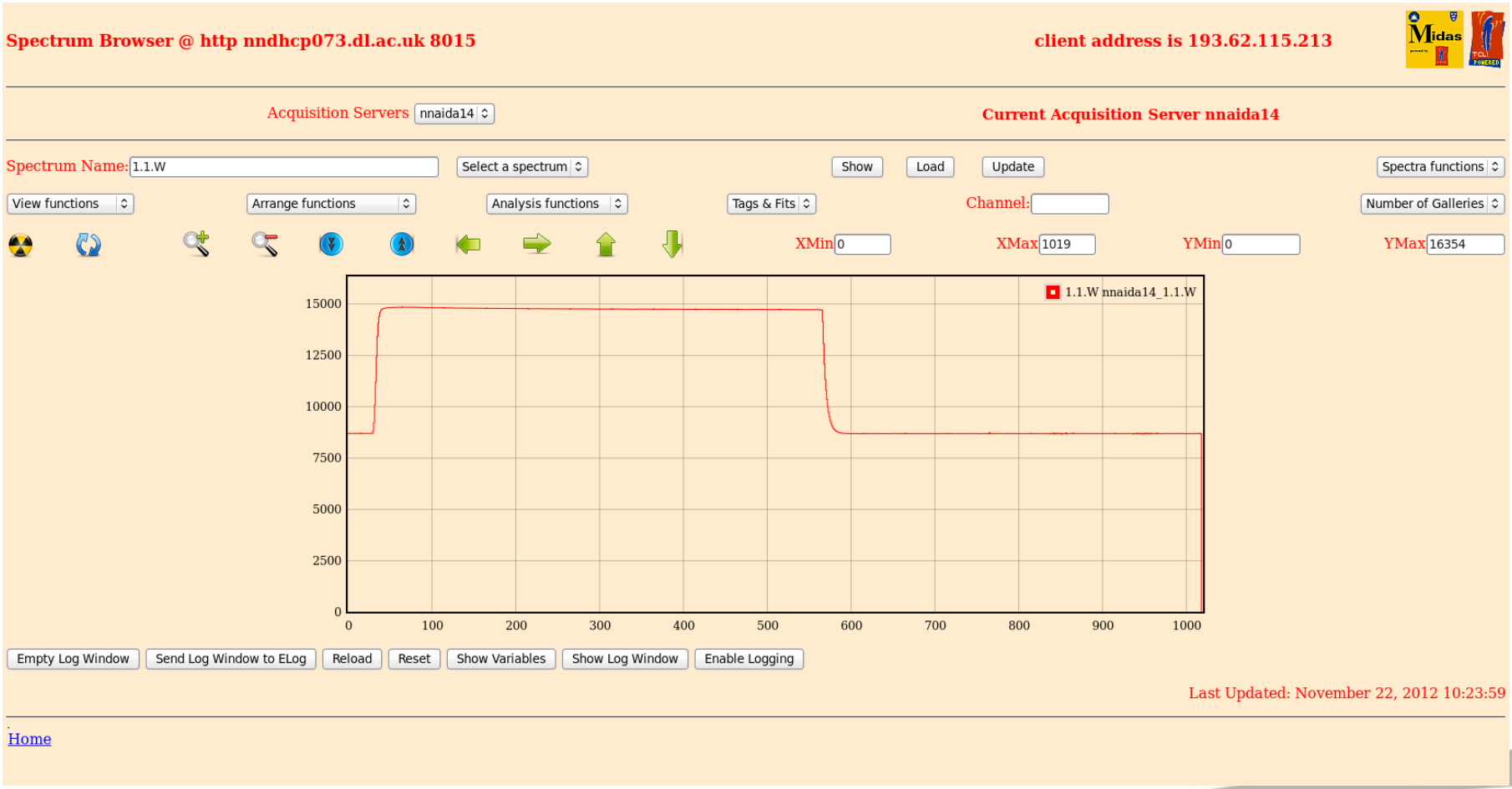
Trace Capture - Trace



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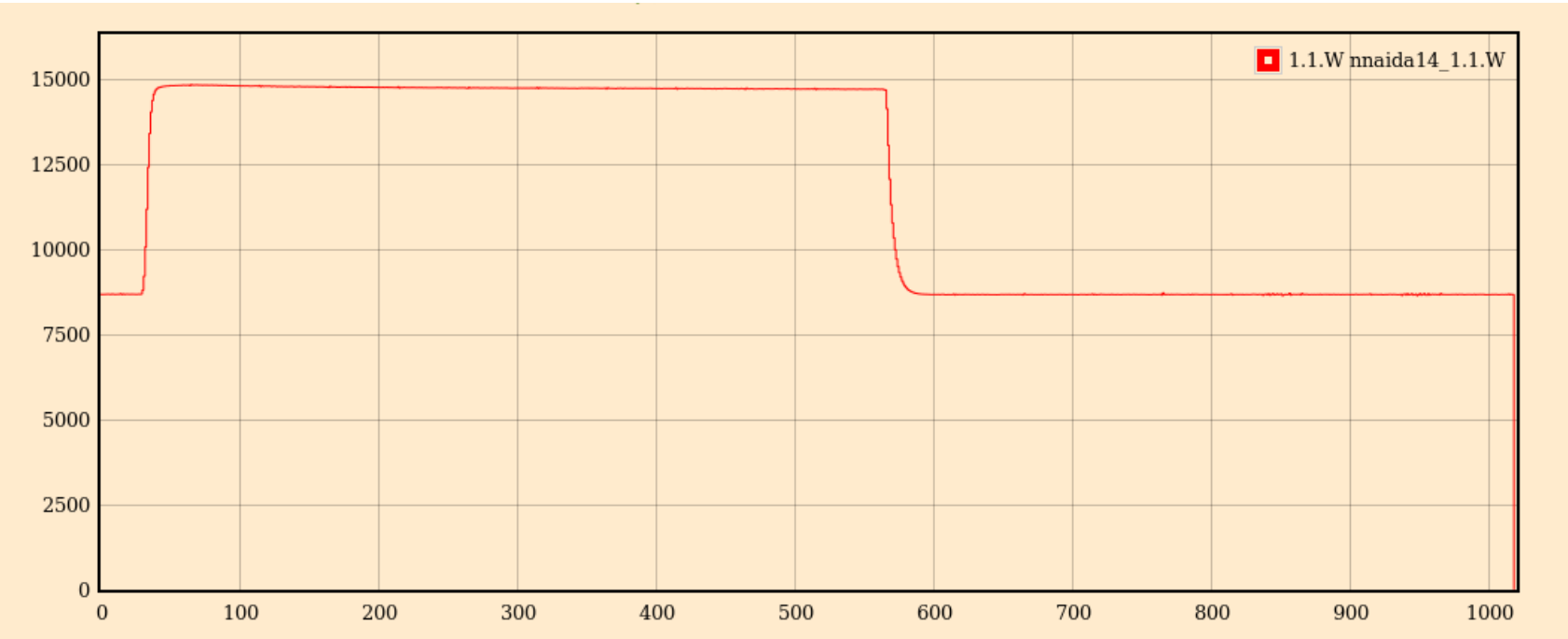
Trace Capture - Trace



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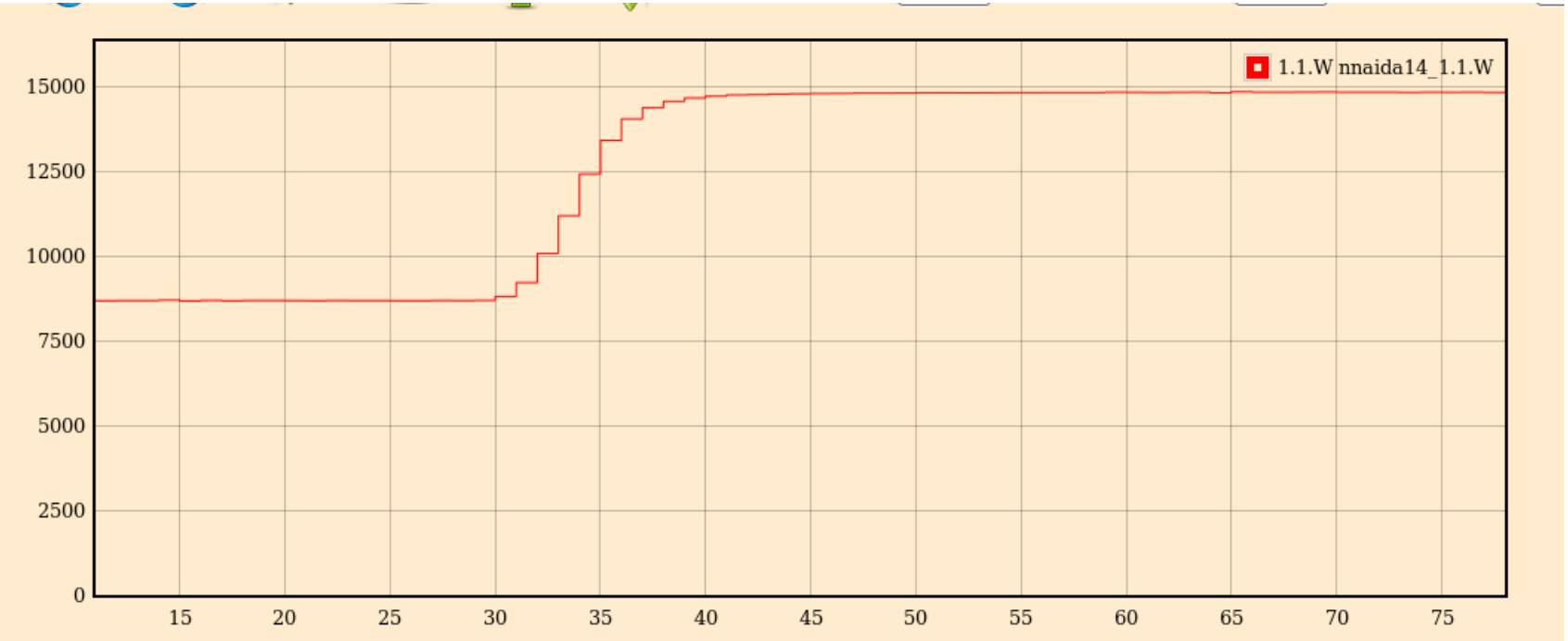
Trace Capture – Trace - zoomed



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Trace Capture - Processing

- Traces are processed as the data passes from the Q8 units to the DMA Transfer unit.
- Currently a CFD is implemented. The Pre_Trigger samples are used to calculate a Baseline, then the CFD algorithm is applied to corrected data. The zero crossing point as an integer and fraction delayed from the LED Timestamp are written over the last two sample values.
- The parameters available are :
  - Number of samples for the Baseline calculation (power of 2). 10 bits.
  - Number of sample clocks for the CFD delay. 4 bits.
  - Two's complement CFD threshold. 16 bits.
  - Fraction. 0x80 ⇔ 0.5. 8 bits.

Post Processing

The AIDA data can currently be written to disc as mixed unsorted data.
To extract information to help with development of the processing algorithm GRAIN sorting software is planned to be used.
A test of the algorithm uses the SYNC pulse from the FEE64 via a MACB to trigger a PB-5 and hence Trace capture and processing.
Panu Rahkila has agreed to help create the Trigger for extracting SYNC pulse associated items.